



AMAS-BT 2010 CALL FOR PAPERS

3rd Workshop on Architectural and Microarchitectural Support for Binary Translation
Held in conjunction with the 37th Int'l Symposium on Computer Architecture (ISCA-37)

Saint-Malo, France -- June 20, 2010

<http://amas-bt.cs.virginia.edu/>

Workshop Organizers

- Mauricio Breternitz, Intel
- Robert Cohn, Intel
- Erik Altman, IBM Research
- Youfeng Wu, Intel

Program Committee

- Erik Altman, IBM Research
- Guido Araujo, UNICAMP
- Mauricio Breternitz, Intel
- Mark Charney, Intel
- Josep M. Codina, Intel
- Robert Cohn, Intel
- Andy Glew, Intel
- Kim Hazelwood, University of Virginia
- David Kaeli, Northeastern University
- Chris J. Newburn, Intel
- Suresh Srinivas, Intel
- Chenggang Wu, CAS, China
- Youfeng Wu, Intel

Important Dates

- Abstracts: April 30, 2010
- Submission: May 9, 2010
- Notification: May 16, 2010

Long employed by industry, large scale use of binary translation and on-the-fly code generation is becoming pervasive both as an enabler for virtualization, processor migration and also as processor implementation technology. The emergence and expected growth of just-in-time compilation, virtualization and Web 2.0 scripting languages brings to the forefront a need for efficient execution of this class of applications. The availability of multiple execution threads brings new challenges and opportunities, as existing binaries need to be transformed to benefit from multiple processors, and extra processing resources enable continuous optimizations and translation.

The main goal of this half-day workshop is to bring together researchers and practitioners with the aim of stimulating the exchange of ideas and experiences on the potential and limits of **Architectural and MicroArchitectural Support for Binary Translation** (hence the acronym AMAS-BT). The key focus is on challenges and opportunities for such assistance and opening new avenues of research. A secondary goal is to enable dissemination of hitherto unpublished techniques from commercial projects.

The workshop scope includes support for decoding/translation, support for execution optimization and runtime support. It will set a high scientific standard for such experiments, and requires insightful analysis to justify all conclusions. The workshop will favor submissions that provide meaningful insights, and identify underlying root causes for the failure or success of the investigated technique. Acceptable work must thoroughly investigate and communicate why the proposed technique performs as the results indicate.

How to Submit

Submit using EasyChair: www.easychair.org/login.cgi?conf=amasbt2010

- abstracts due by April 30, 2010
- publication-ready submission of less than 5000 words in IEEE style, 2-column, 10-point .doc, .pdf, or .ps format, due by May 9, 2010

Submission Topics

Binary translation: architectural effects and experience

- Novel applications of binary translation and virtualization
- Performance characterization
- Dynamic instrumentation and debugging
- HW/SW co-design for efficient execution
- Experimental insights on binary translation and industrial experience

Hardware assistance for translation and code discovery

- Interpretation, decoding assistance, code dispatch
- On-the-fly reconstruction of CFGs and data dependences, scheduling and optimization
- Bug-per-bug compatibility issues
- Static translation with/without runtime assistance/translation (hybrid translation)

Hardware assistance for runtime management

- Self-modifying or self-referential code, precise exceptions
- Runtime profiling: branches, caches, memory accesses
- Management of translated code
- Adapting code to changing program behavior
- Persistent translation, incremental translation
- Parallel translation, auto parallelization, speculation

Hardware assistance for optimization

- Extra/enhanced internal/physical registers
- Speculative execution support
- Reduced footprint/low-power cores enabled by binary translation, area and power efficiency
- Techniques for parallelizing single-thread programs